Amendments to the Claims:

Listing of Claims:

Claims 1-11 (cancelled)

Claim 12 (original) A flash memory cell comprising:

a substrate;

a stacked gate structure positioned on the substrate, wherein the stacked gate structure from bottom to top comprises a tunneling oxide, a floating gate, an insulating layer, and a control gate, the floating gate and the control gate having an insulating barrier layer with rounded edges;

a first conductive type shallow doped region positioned in the substrate under the stacked gate structure;

a first conductive type deep region positioned in the substrate at one side of the stacked gate structure;

a second conductive type drain doped region positioned in the substrate at a same side with the deep doped region, a bottom and sidewalls of the drain doped region being surrounded by the deep doped region; and

a second conductive type source doped region positioned in the substrate at an opposite side of the stacked gate structure.

Claim 13 (original) The flash memory cell of claim 12 wherein the substrate further comprises a second conductive type well, and the shallow doped region, the deep doped region, the drain doped region, and the source doped region are positioned above the second conductive type well.

Claim 14 (original) The flash memory cell of claim 12 wherein the first conductive type is P type and the second conductive type is N

type.

Claim 15 (original) The flash memory cell of claim 12 wherein the control gate further comprises a silicide layer thereon.

Claim 16 (original) The flash memory cell of claim 12 wherein the stacked gate structure further comprises a TEOS layer thereon.

Claim 17 (original) The flash memory cell of claim 12 wherein the insulating layer is an oxide layer.

Claim 18 (original) The flash memory cell of claim 12 wherein the insulating barrier layer composite-layer structure comprises at least an oxide layer and at least a nitride layer.

Claim 19 (original) The flash memory cell of claim 12 wherein the insulating layer is an ONO (oxide-nitride-oxide) layer.

Claim 20 (original) The flash memory cell of claim 12 wherein the drain doped region and the deep doped region are electrically connected together.